

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
-40V	25mΩ@-10V	-16A
	35mΩ@-4.5V	

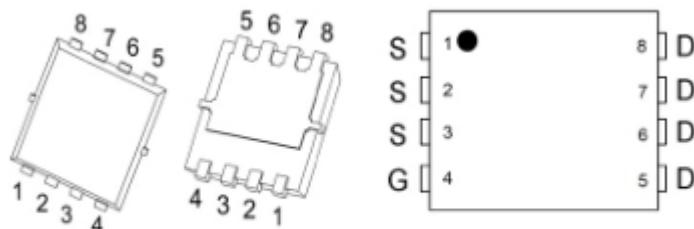
Feature

- TrenchFET Power MOSFET
- Excellent RDS(on) and Low Gate Charge

Applications

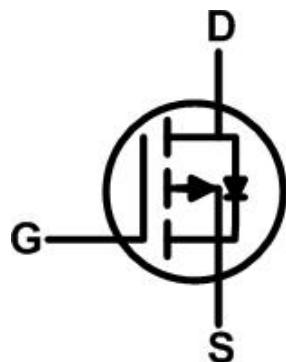
- Advanced trench process technology
- High density cell design for ultra-low on-resistance
- High power and current handing capability
- Ideal for Lion battery pack applications

Package

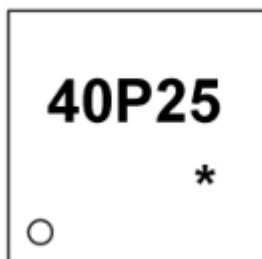


PDFNWB3.3×3.3-8L

Circuit diagram



Marking



40P25 = Device Code
* = Month Code

Absolute maximum ratings

($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	-16	A
Pulsed Drain Current ²	I_{DM}	-64	A
Power Dissipation ³	P_D	28	W
Thermal Resistance from Junction to Ambient ¹	$R_{\theta JA}$	4.4	$^\circ\text{C}/\text{W}$
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 To 150	$^\circ\text{C}$

Electrical characteristics

($T_A=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$\text{BV}_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32\text{V}, V_{GS} = 0\text{V}$			-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	μA
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.2	-1.5	-2.2	V
Drain-Source On-Resistance	$R_{DS(\text{on})}$	$V_{GS} = -10\text{V}, I_D = -5\text{A}$		25	35	$\text{m}\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -4\text{A}$		35	50	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{V}, I_D = -8\text{A}$		12		S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		2700		pF
Output Capacitance	C_{oss}			370		
Reverse Transfer Capacitance	C_{rss}			310		
Switching Characteristics						
Total Gate Charge@-4.5V	Q_g	$V_{DS} = -15\text{V}, I_D = -4.5\text{A}, I_D = -1\text{A}$		11.5		nC
Gate-Source Charge	Q_{gs}			3.5		
Gate-Drain Charge	Q_{gd}			3.3		
Turn-on Delay Time	$T_{d(on)}$	$V_{DD} = -15\text{V}, V_{GS} = -10\text{V}, R_G = 3\Omega, I_D = -1\text{A}$		22		nS
Turn-on Rise Time	T_r			15.7		
Turn-off Delay Time	$T_{d(off)}$			59		
Turn-off Fall Time	T_f			5.5		
Drain-Source Diode Characteristics						
Continuous Source Current ^{1,4}	I_s	$V_G = V_D = 0\text{V}$, Force Current			-8	A
Diode Forward Voltage	V_{SD}	$V_{GS} = 0\text{V}, I_s = -1\text{A}, T_j = 25^\circ\text{C}$			-1.2	V

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
3. The power dissipation is limited by 150°C junction temperature
4. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

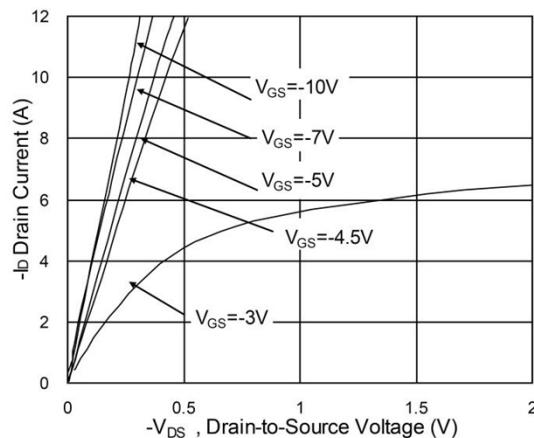


Fig.1 Typical Output Characteristics

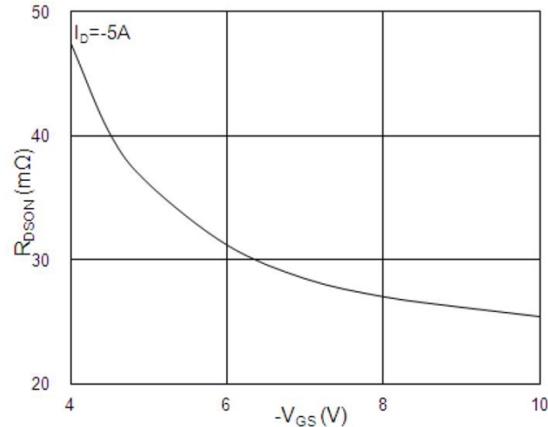


Fig.2 On-Resistance vs. Gate-Source Voltage

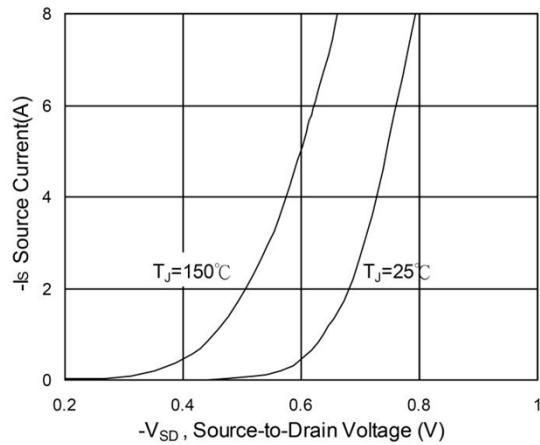


Fig.3 Forward Characteristics of Reverse

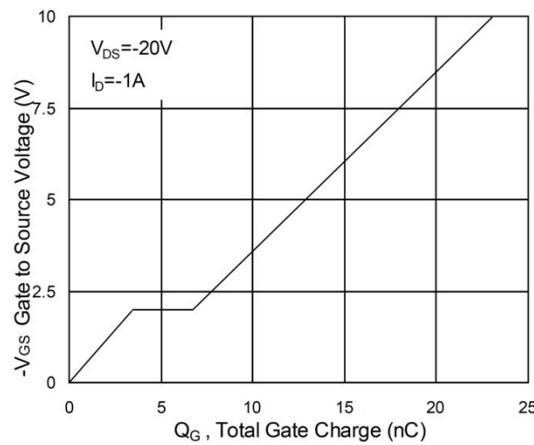


Fig.4 Gate Charge Characteristics

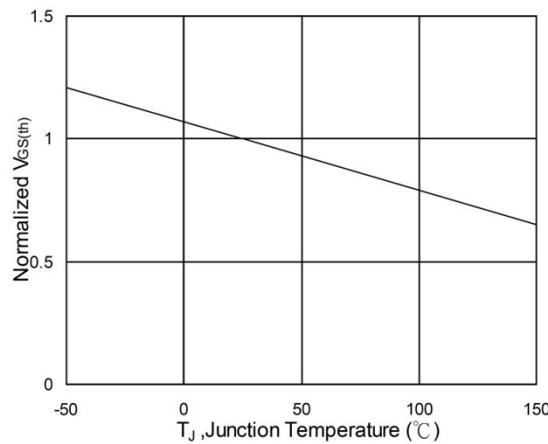


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

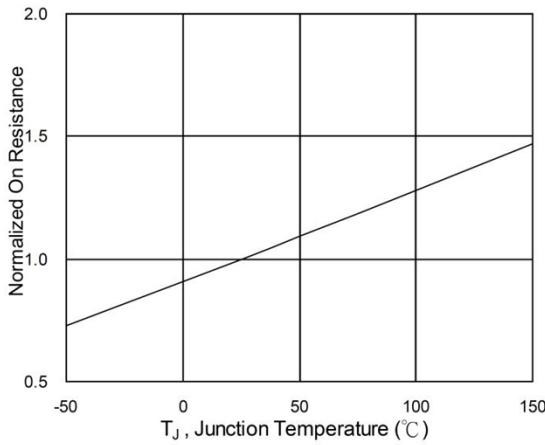
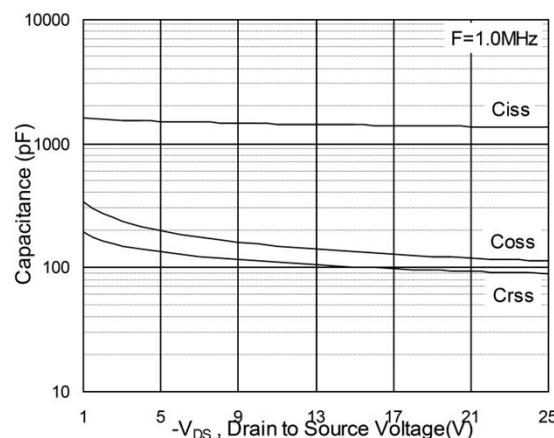
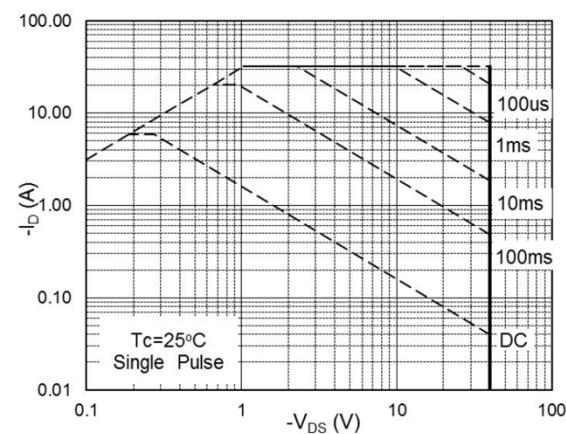
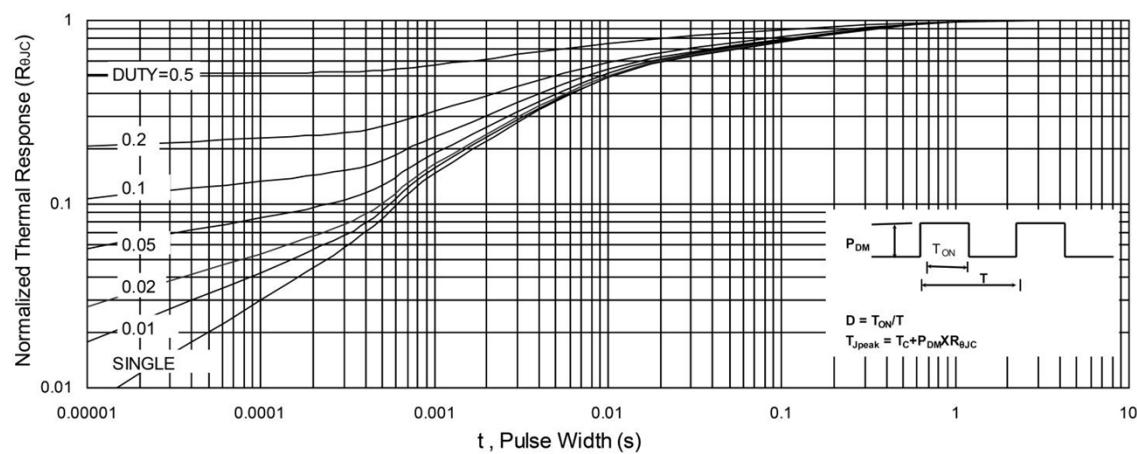
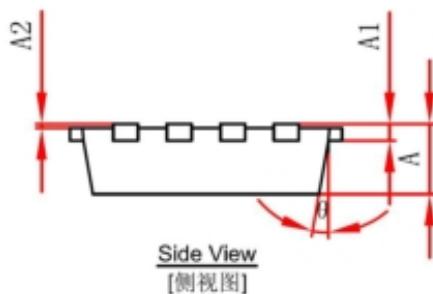
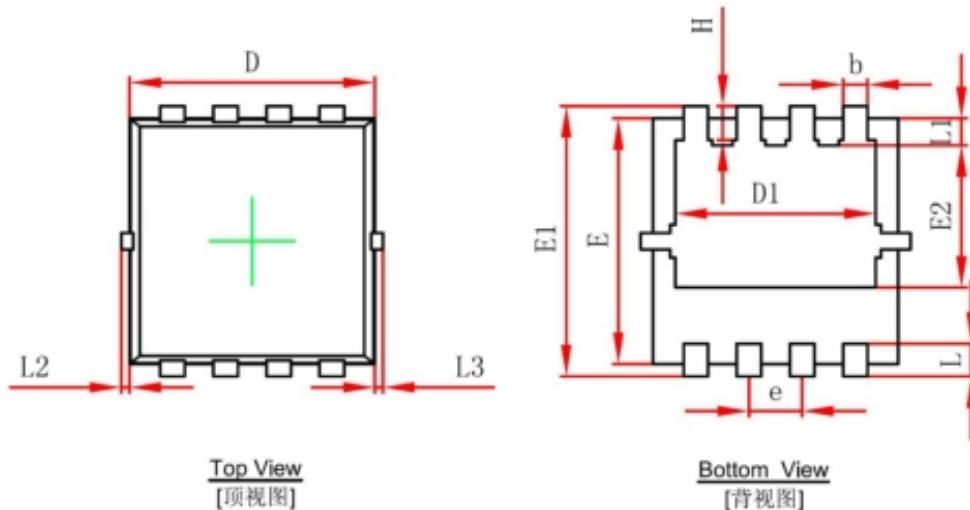


Fig.6 Normalized $R_{DS(on)}$ vs. T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

PDFNWB3.3×3.3-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.			0.006 REF.
A2	0~0.05			0~0.002
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100			0~0.004
L3	0~0.100			0~0.004
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°