Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
-40V	10mΩ@-10V	-33A
	14mΩ@-4.5V	

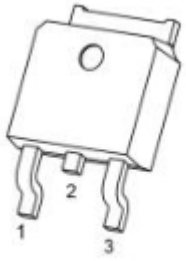
Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

Applications

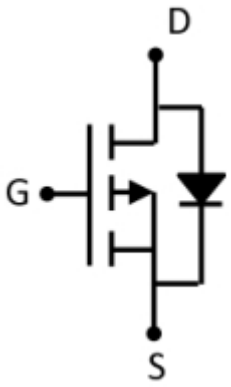
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package



TO-252-2L(G:1 D:2 S:3)

Circuit diagram



Marking

40P10 : Product code
** : Week code.

Absolute maximum ratings

(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-33	A
Drain Current-Continuous(T_C=100℃)	$I_{D(100℃)}$	-23	
Pulsed Drain Current	I_{DM}	-132	A
Maximum Power Dissipation	P_D	52	W
Single pulse avalanche energy (1)	E_{AS}	544	mJ
Thermal Resistance,Junction-to-Case(2)	$R_{\theta JC}$	2.4	℃/W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	℃

Electrical characteristics

(T_A=25℃, unless otherwise noted)

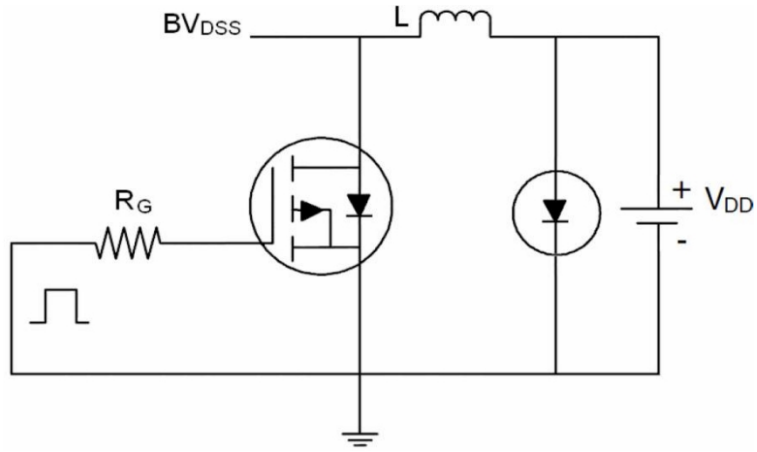
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$BV_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =-40V, V_{GS} = 0V			-1	uA
Gate-Source Leakage	I_{GSS}	V_{GS} =±20V, V_{DS} =0V			±100	uA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-1.0	-1.5	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} =-10V, I_D =-12A		10	13	mΩ
		V_{GS} =-4.5V, I_D =-10A		14	20	
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz		3500		pF
Output Capacitance	C_{oss}			323		
Reverse Transfer Capacitance	C_{rss}			222		
Switching Characteristics						
Turn-on Delay Time	$T_{d(on)}$	V_{DD}=-20V, I_D=-1A , V_{GS}=-10V, R_G=6Ω		12		nS
Turn-on Rise Time	T_r			25		
Turn-off Delay Time	$T_{d(off)}$			30		
Turn-off Fall Time	T_f			24		
Total Gate Charge	Q_g	V_{DS} =-20V, , I_D=-25A V_{GS}=-10V		72		nC
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			15		
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-12A			-1.2	V

Notes:

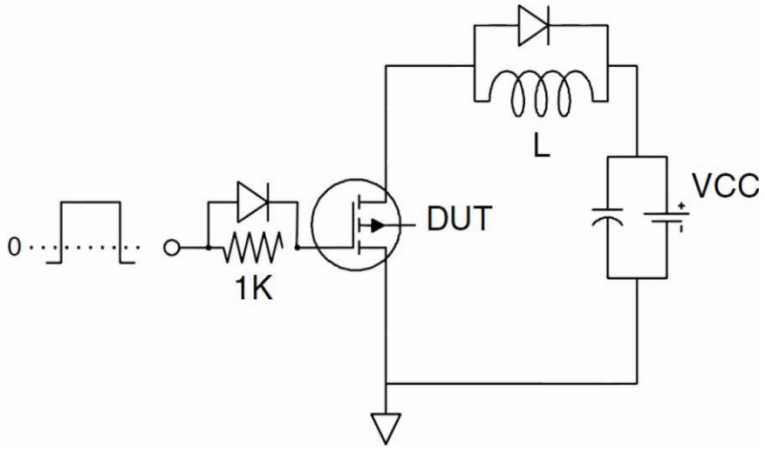
1. E AS condition:T_j=25℃,V_{DD} =-25V,V_{GS} =-10V,L=0.1mH,I_{AS} =-54A
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuits

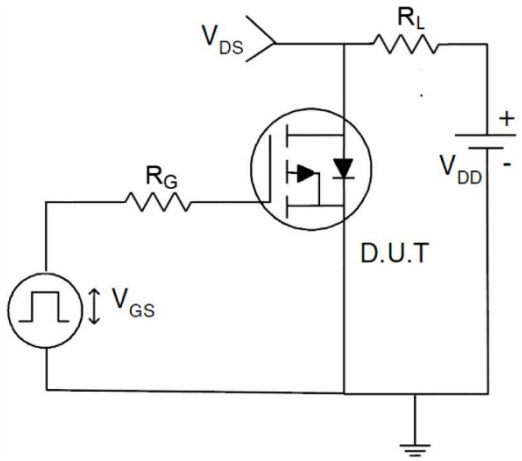
- EAS Test Circuits



- Gate Charge Test Circuit



- Switch Time Test Circuit



Typical Characteristics

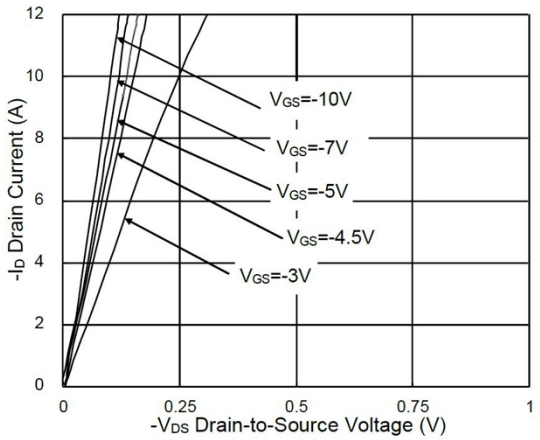


Fig.1 Typical Output Characteristics

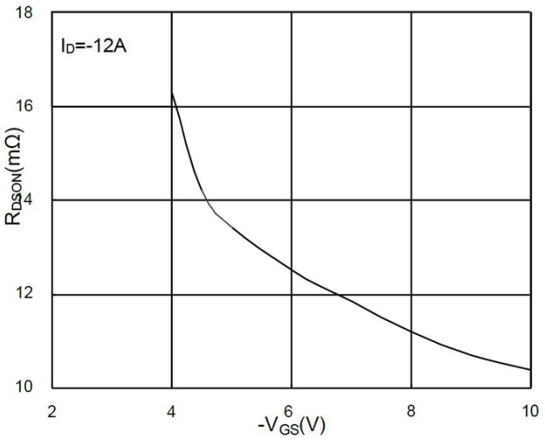


Fig.2 On-Resistance v.s Gate-Source

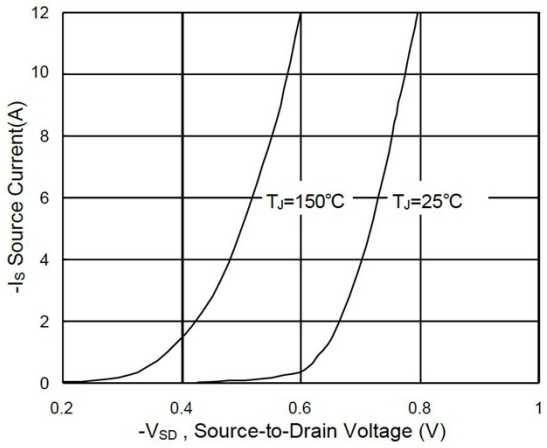


Fig.3 Forward Characteristics Of Reverse

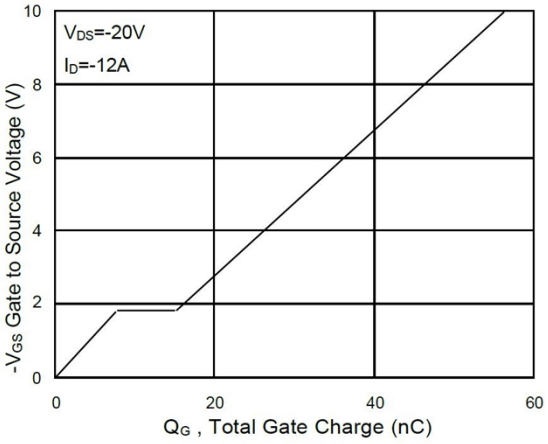


Fig.4 Gate-Charge Characteristics

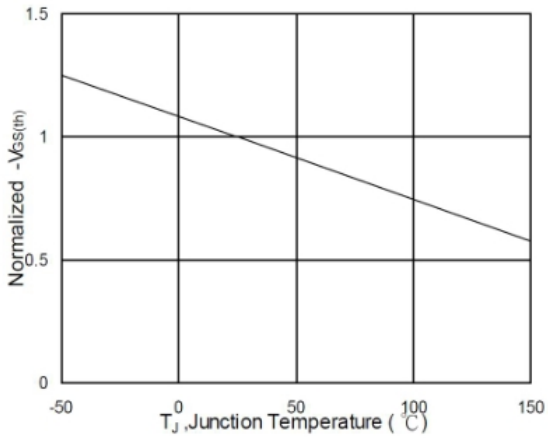


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

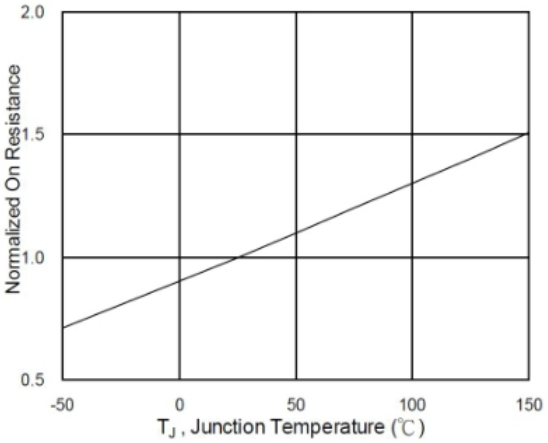


Fig.6 Normalized R_{DSON} v.s T_J

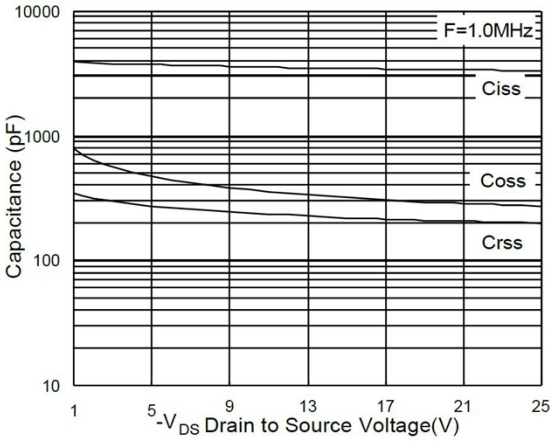


Fig.7 Capacitance

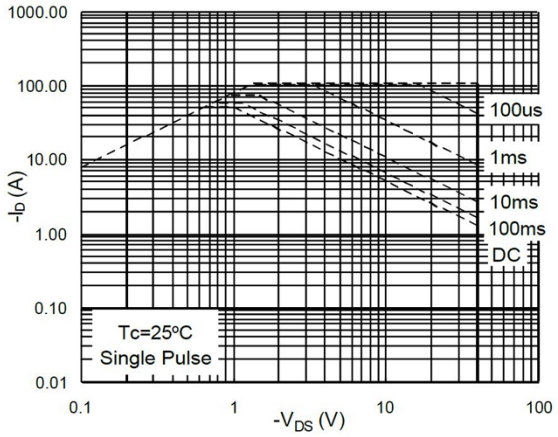


Fig.8 Safe Operating Area

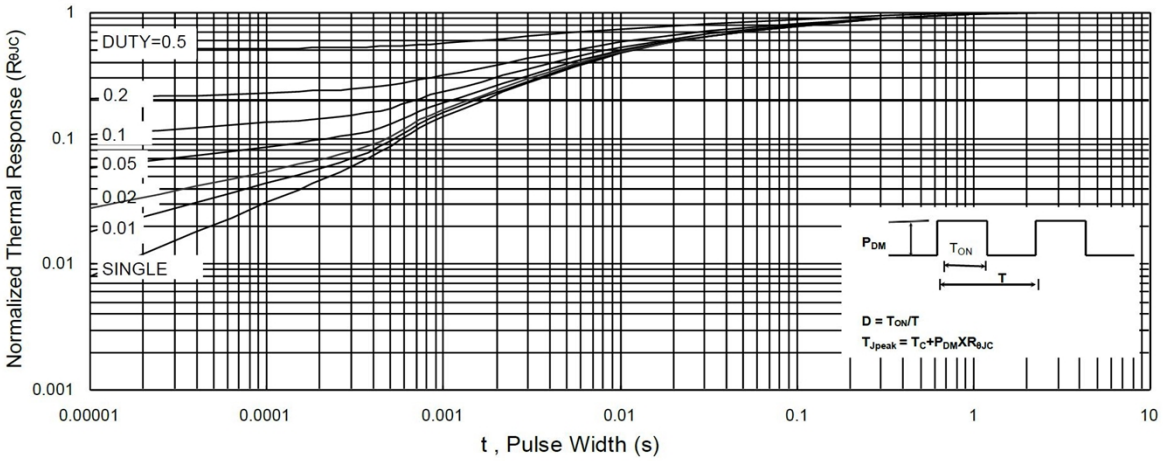


Fig.9 Normalized Maximum Transient Thermal Impedance

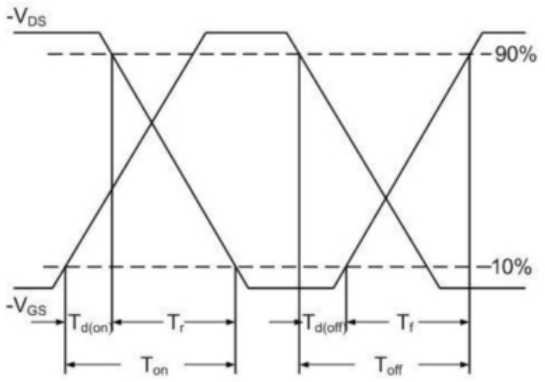


Fig.10 Switching Time Waveform

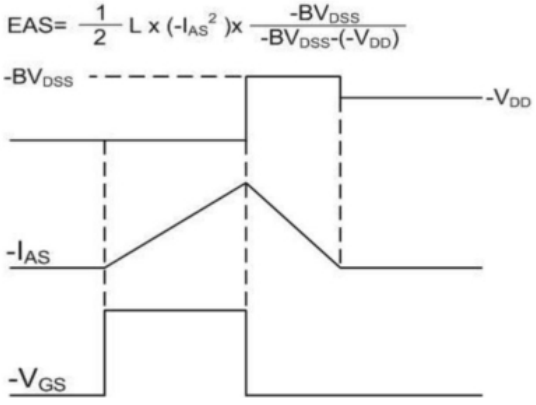
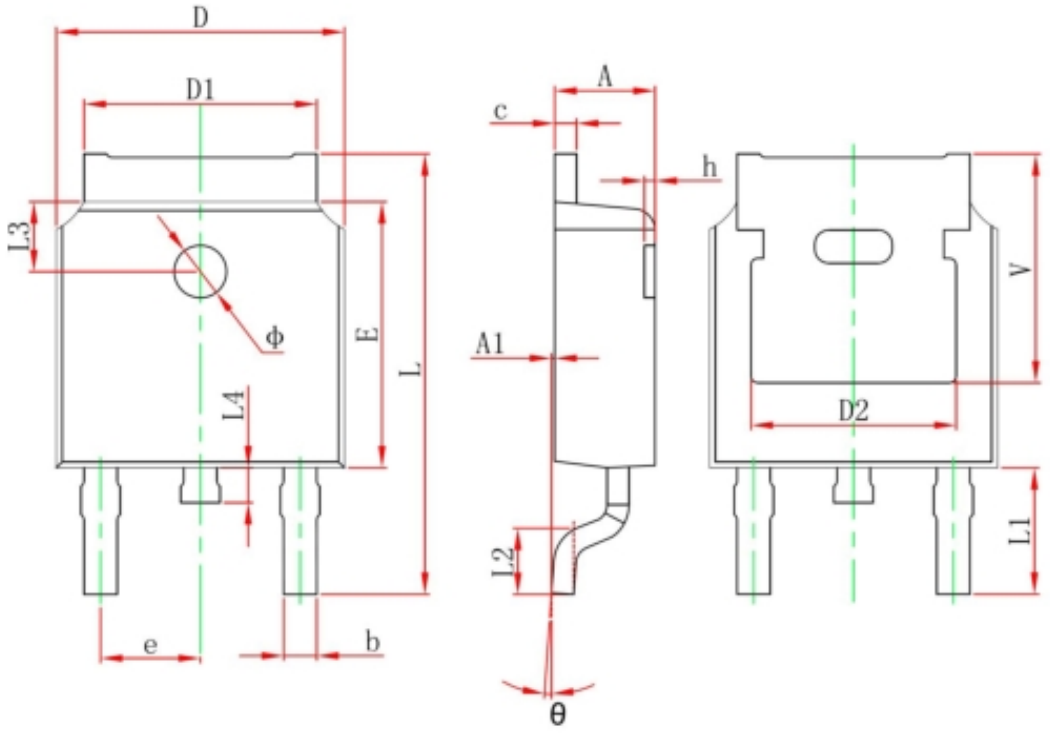


Fig.11 Unclamped Inductive Waveform

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	