

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	$I_D$
-40V	8.6mΩ@-10V	-45A
	13mΩ@4.5V	

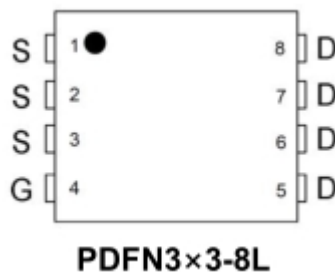
## Feature

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation

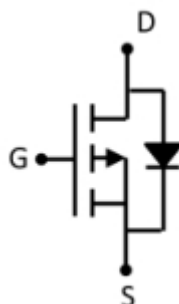
## Applications

- Power switching application
- PWM Application
- DC-DC Converter

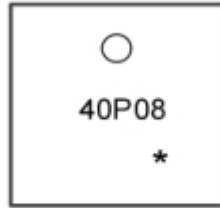
## Package



## Circuit diagram



## Marking



40P08 : Product code  
\* : Month code

## Absolute maximum ratings

(T<sub>a</sub>=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	-40	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	-45	A
Pulsed Drain Current	I <sub>DM</sub>	-180	A
Maximum Power Dissipation (T <sub>c</sub> =25°C)	P <sub>D</sub>	80	W
Single pulse avalanche energy <sup>1</sup>	E <sub>AS</sub>	600	mJ
Thermal Resistance, Junction-to-Case <sup>2</sup>	R <sub>θJC</sub>	1.56	°C/W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

## Electrical characteristics

( $T_A=25^{\circ}\text{C}$ , unless otherwise noted)

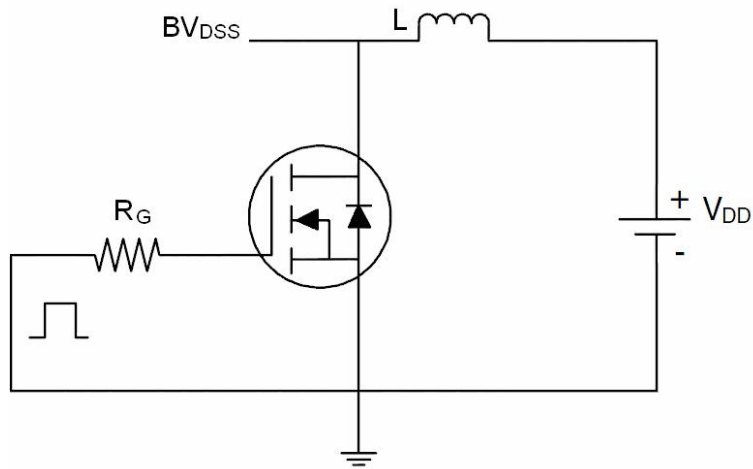
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-Source Breakdown Voltage	$BV_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -40V, V_{GS} = 0V$			-1	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V, V_{DS} = 0V$			$\pm 100$	$\mu A$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.2	-1.6	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -10A$		8.6	11	m $\Omega$
		$V_{GS} = -4.5V, I_D = -8A$		13	18	
Dynamic Characteristics						
Input Capacitance	$C_{iss}$	$V_{GS}=0V, V_{DS}= -20V,$ $f=1MHz$		4004		pF
Output Capacitance	$C_{oss}$			309		
Reverse Transfer Capacitance	$C_{rss}$			229		
Switching Characteristics						
Turn-on Delay Time	$T_{d(on)}$	$V_{DD}= -20V, I_D= -10A,$ $V_{GS}= -10V, R_G=3\Omega$		9.9		nS
Turn-on Rise Time	$T_r$			32		
Turn-off Delay Time	$T_{d(off)}$			46		
Turn-off Fall Time	$T_f$			53		
Total Gate Charge ( $V_{GS}= -4.5V$ )	$Q_g$	$V_{DS} = -20V, , I_D= -20A$ $V_{GS}= -10V$		31		nC
Total Gate Charge ( $V_{GS}= -10V$ )	$Q_g$			67		
Gate-Source Charge	$Q_{gs}$			13.2		
Gate-Drain Charge	$Q_{gd}$			11		
Drain-Source Diode Characteristics						
Diode Forward Voltage	$V_{SD}$	$V_{GS}=0V, I_S= -60A$			-1.2	V

### Note:

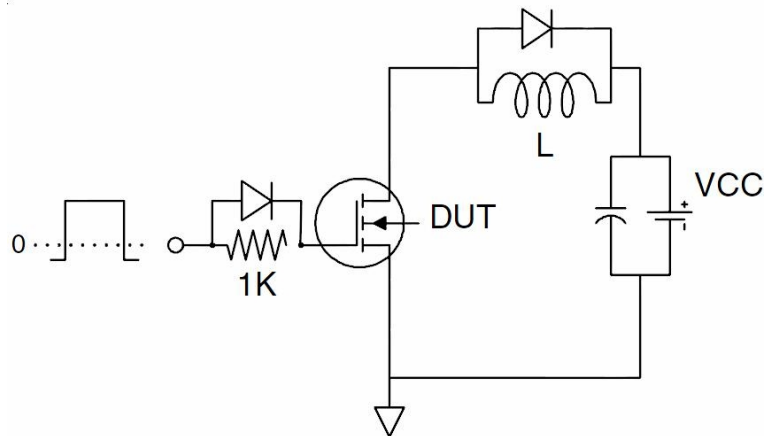
1.  $E_{AS}$  condition:  $T_j=25^{\circ}\text{C}, V_{DD} = -20V, V_G = -10V, L=1mH, R_g = 25\Omega$
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.

## Test Circuits

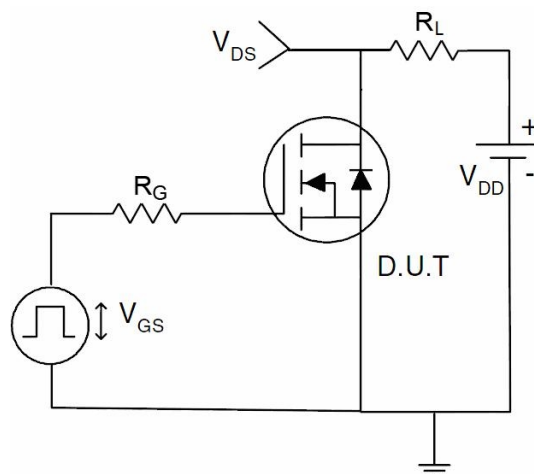
- EAS Test Circuits



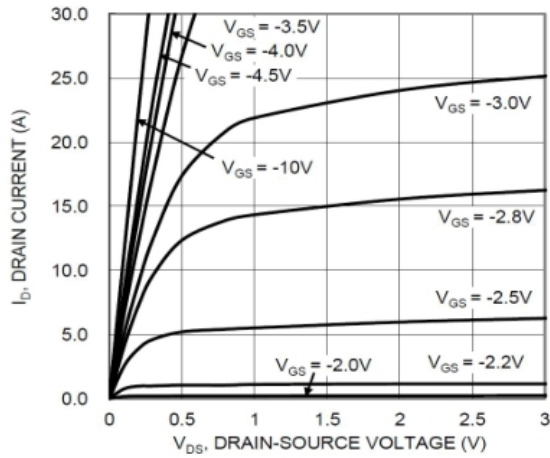
- Gate Charge Test Circuit



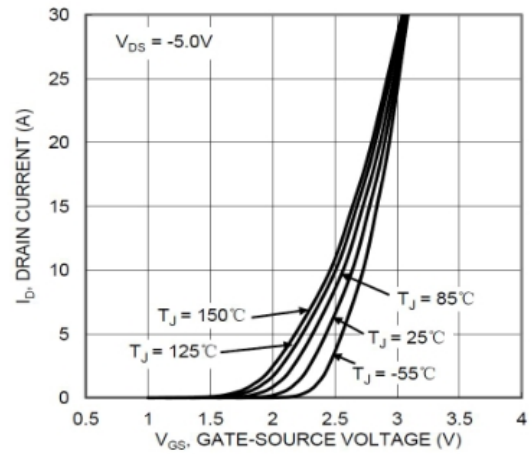
- Switch Time Test Circuit



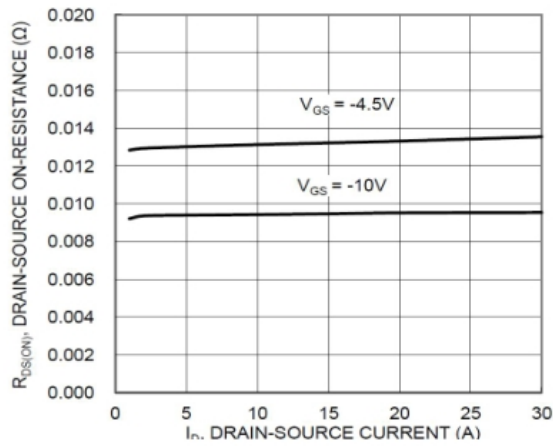
## Typical Characteristics



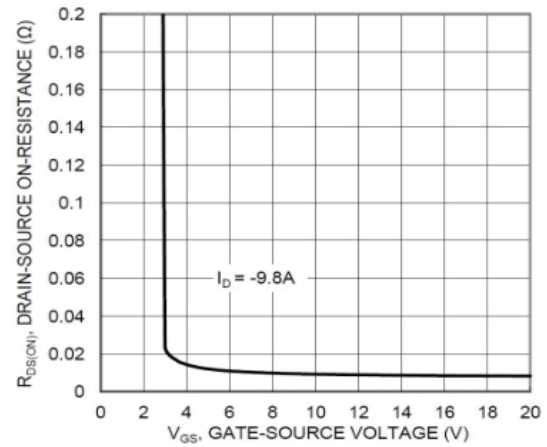
Typical Output Characteristic



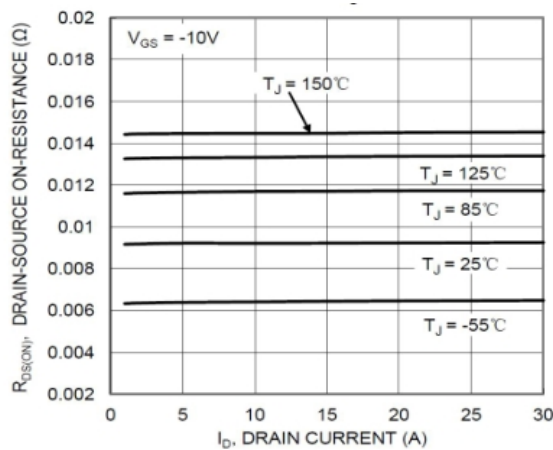
Typical Transfer Characteristic



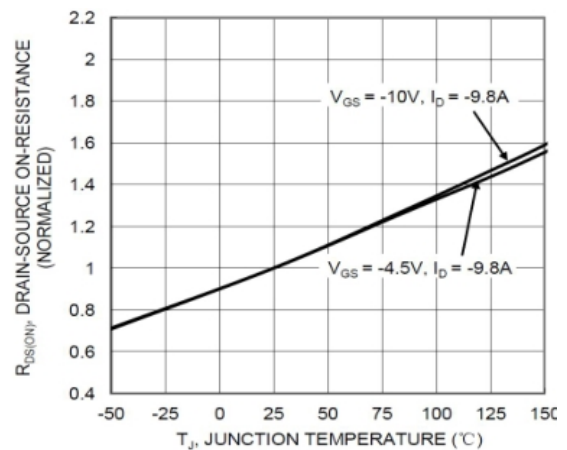
Typical On-Resistance vs. Drain Current and Gate Voltage



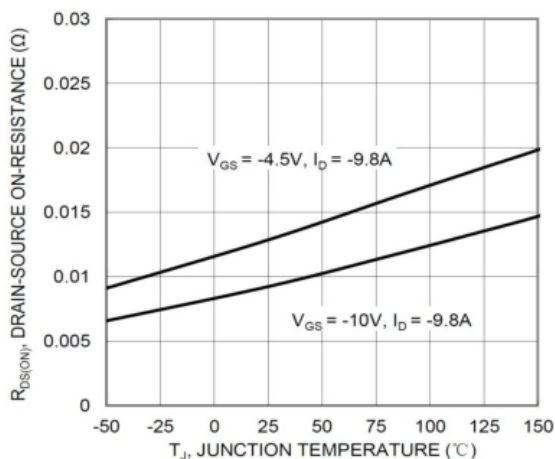
Typical Transfer Characteristic



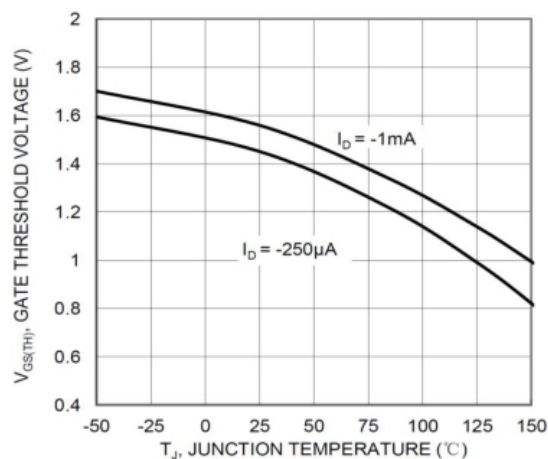
Typical On-Resistance vs. Drain Current and Temperature



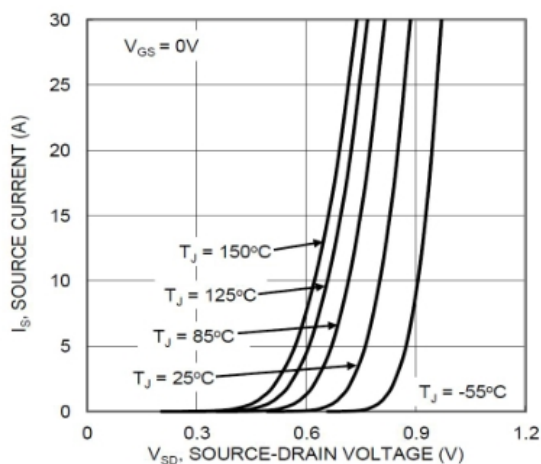
On-Resistance Variation with Temperature



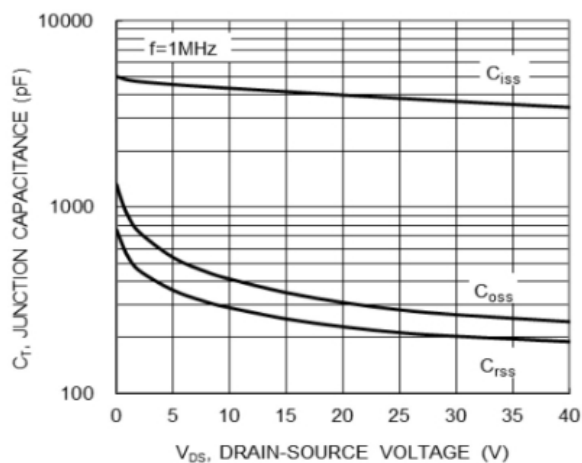
On-Resistance Variation with Temperature



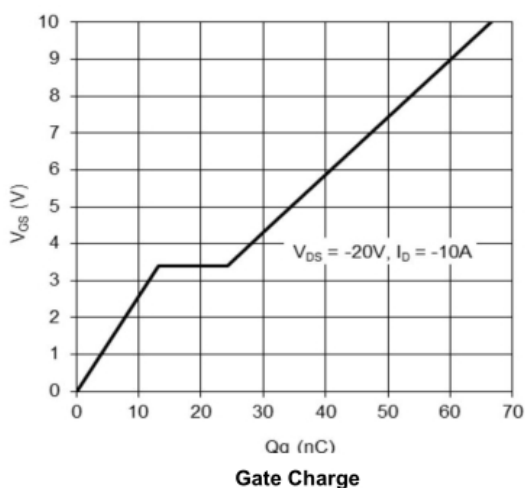
Gate Threshold Variation vs. Junction Temperature



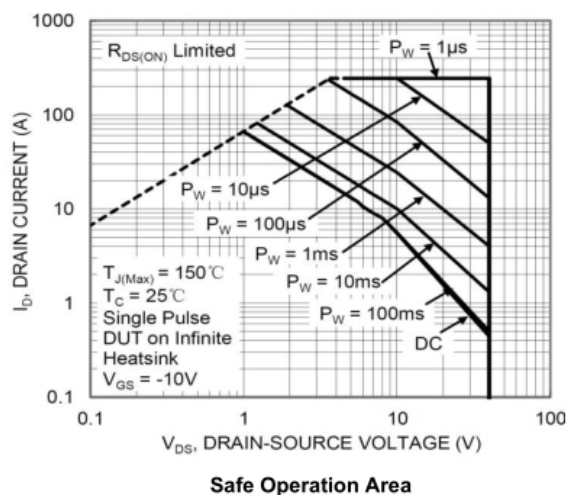
Diode Forward Voltage vs. Current



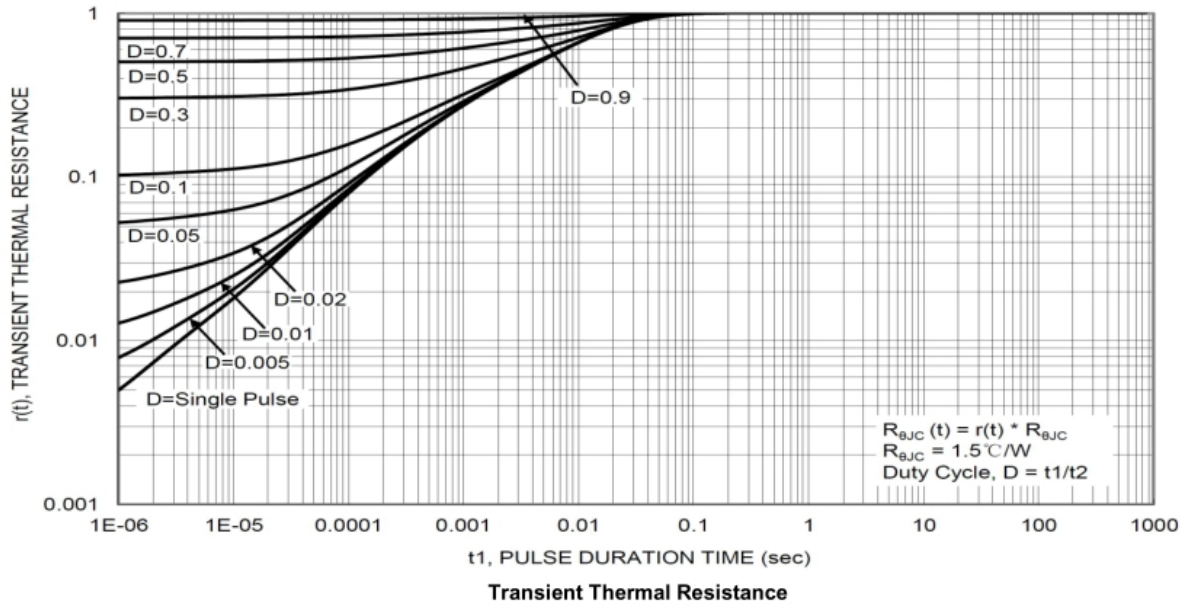
Typical Junction capacitance



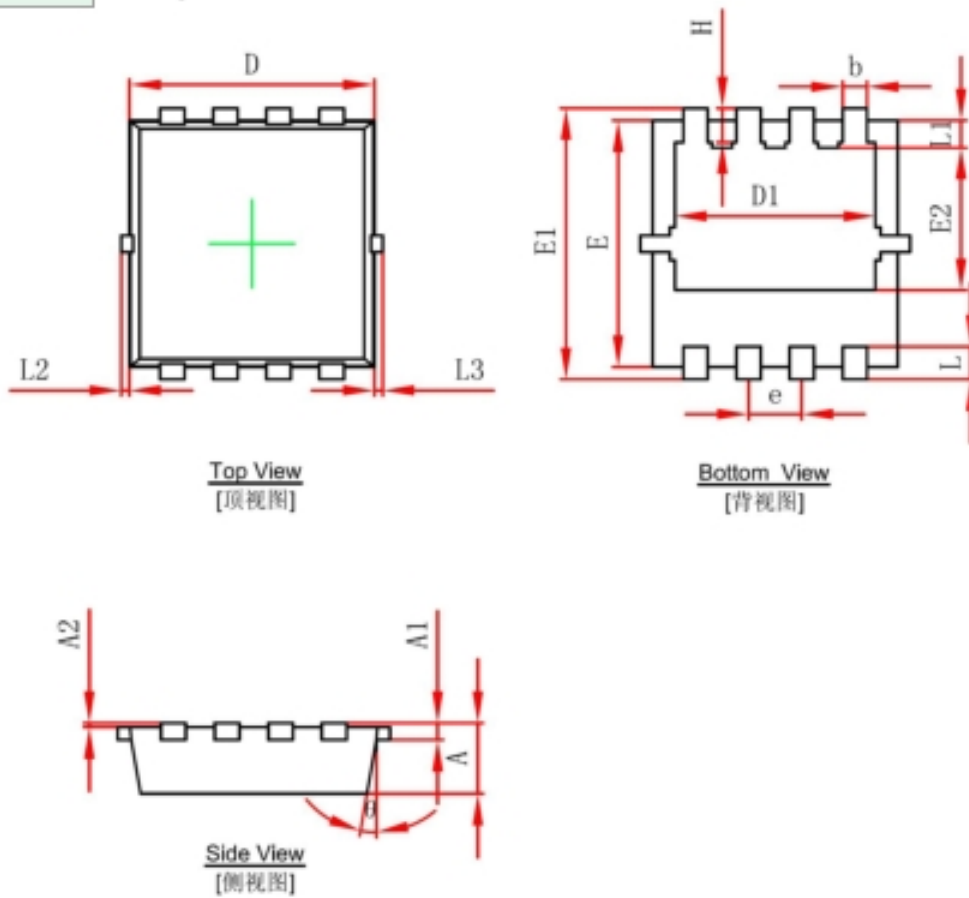
Gate Charge



Safe Operation Area



## PDFN3×3-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°