

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
40V	8mΩ@10V	30A
	11mΩ@4.5V	

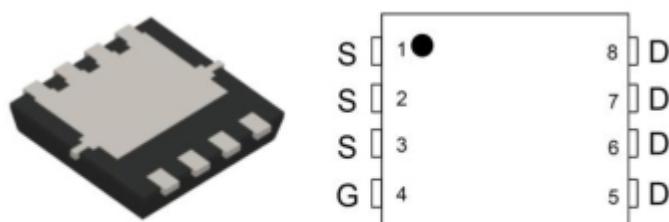
Feature

- $V_{DS} = 40V, I_D = 30A$
- $R_{DS(ON)} < 12m\Omega$ @ $V_{GS}=10V$ (Typ. 8 mΩ)
- $R_{DS(ON)} < 18m\Omega$ @ $V_{GS}=4.5V$ (Typ. 11 mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

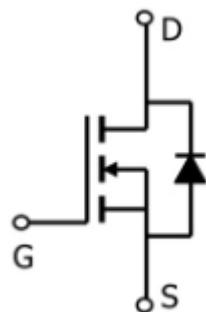
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

Package

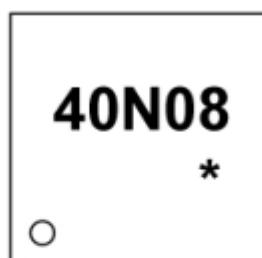


PDFNWB3.3x3.3-8L

Circuit diagram



Marking



40N08 : Product code
* : Month code

Absolute maximum ratings

($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	30	A
Pulsed Drain Current	I_{DM}	120	A
Maximum Power Dissipation	P_D	3	W
Thermal Resistance, Junction-to-Ambient ⁽¹⁾	$R_{\theta JA}$	41.7	$^\circ\text{C}/\text{W}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Electrical characteristics

($T_A=25^\circ\text{C}$, unless otherwise noted)

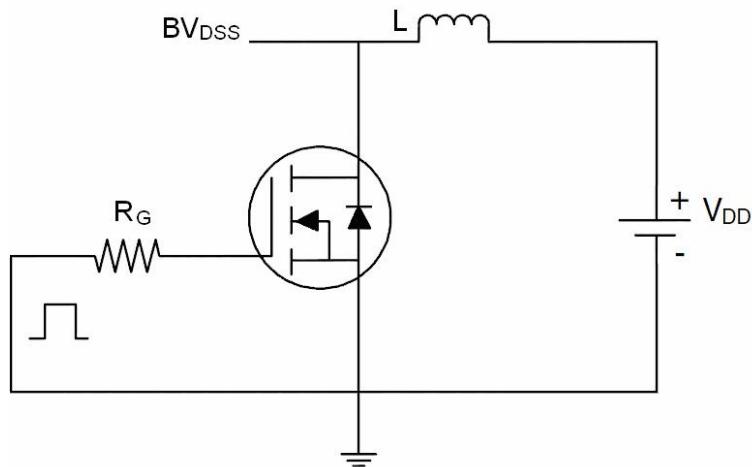
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	$\text{BV}_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	40	45		V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			± 100	μA
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10\text{V}, I_D = 10\text{A}$		8	12	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 8\text{A}$		11	18	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{V}, I_D = 10\text{A}$		75		S
Dynamic Characteristics⁽³⁾						
Input Capacitance	C_{iss}	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1200		pF
Output Capacitance	C_{oss}			124		
Reverse Transfer Capacitance	C_{rss}			58		
Switching Characteristics⁽³⁾						
Turn-On Delay Time	$T_{d(on)}$	$V_{DD} = 20\text{V}, R_L = 2\Omega, V_{GS} = 10\text{V}, R_G = 3\Omega$		6.4		nS
Rise Time	T_r			17.2		
Turn-Off Delay Time	$T_{d(off)}$			29.6		
Fall Time	T_f			16.8		
Total Gate Charge	Q_g	$V_{DS} = 20\text{V}, I_D = 10\text{A}, V_{GS} = 10\text{V}$		30		pF
Gate-Source Charge	Q_{gs}			4.2		
Gate-Drain Charge	Q_{gd}			9.5		
Diode Characteristics						
Diode Forward Voltage ⁽²⁾	V_{SD}	$V_{GS} = 0\text{V}, I_S = 10\text{A}$			1.2	V
Diode Forward Current ⁽¹⁾	I_S				12	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 10\text{A}$ $di/dt = 100\text{A}/\mu\text{s}^{(2)}$		29		nS
Reverse Recovery Charge	Q_{rr}			26		nC

Notes:

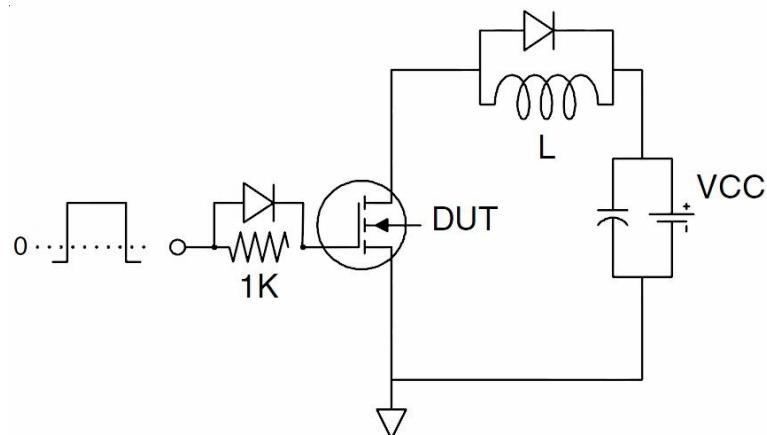
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leqslant 10$ sec.
3. Pulse Test: Pulse Width $\leqslant 300\mu\text{s}$, Duty Cycle $\leqslant 2\%$.
4. Guaranteed by design, not subject to production

Test Circuits

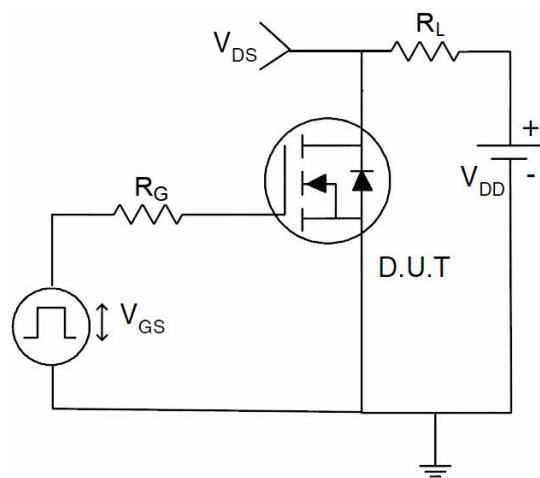
- EAS Test Circuits



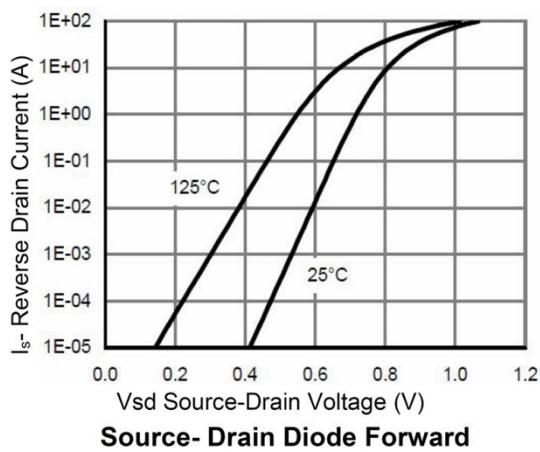
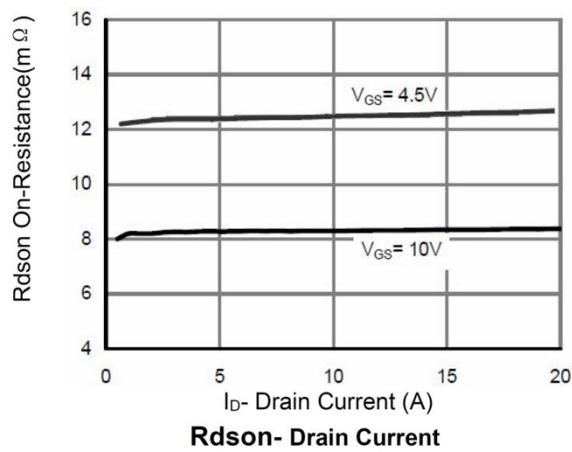
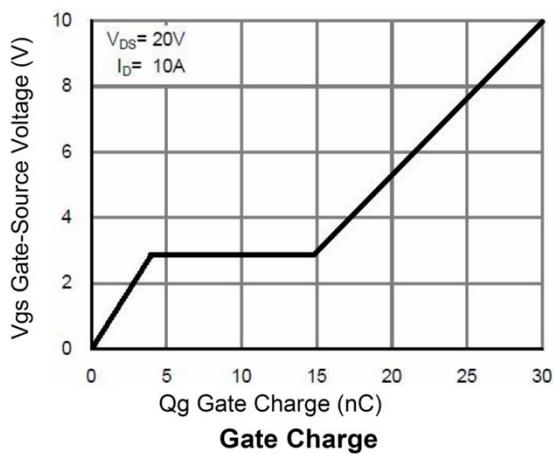
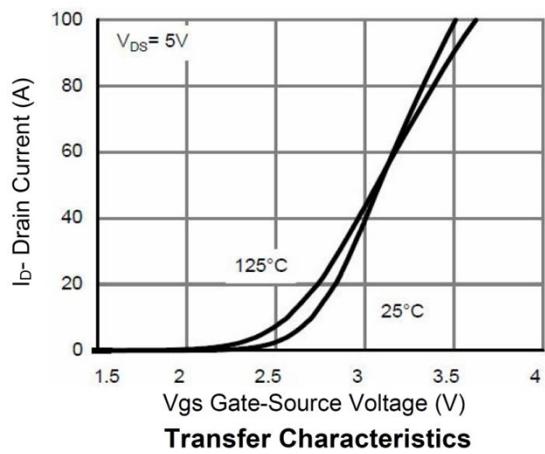
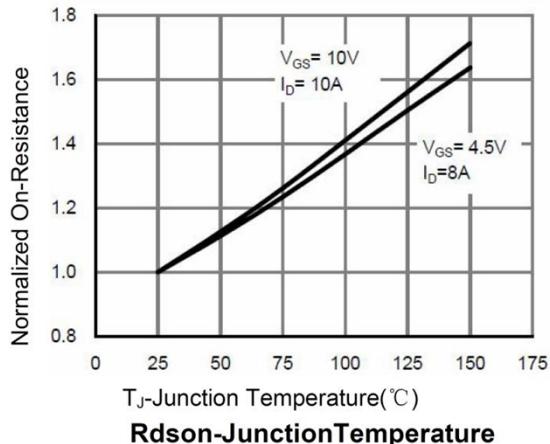
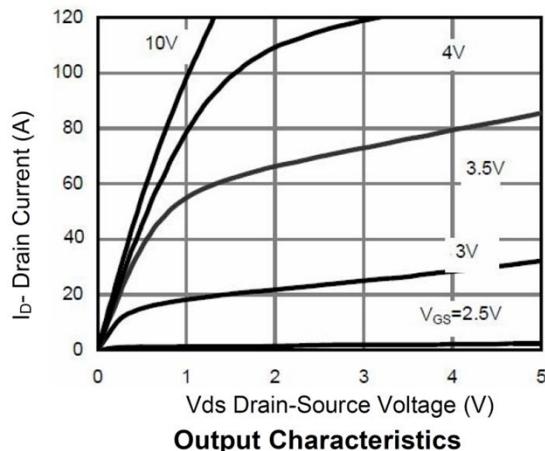
- Gate Charge Test Circuit

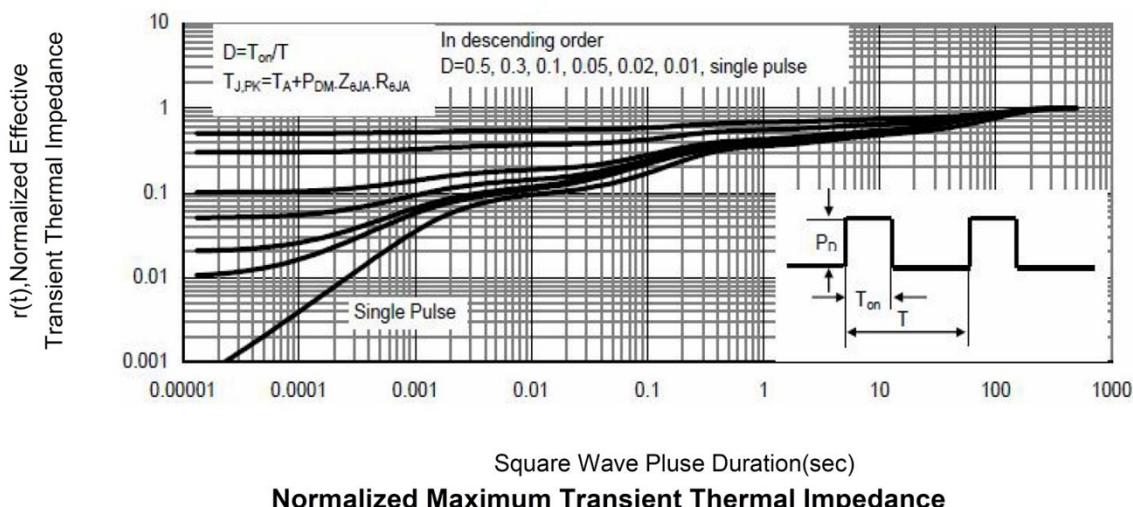
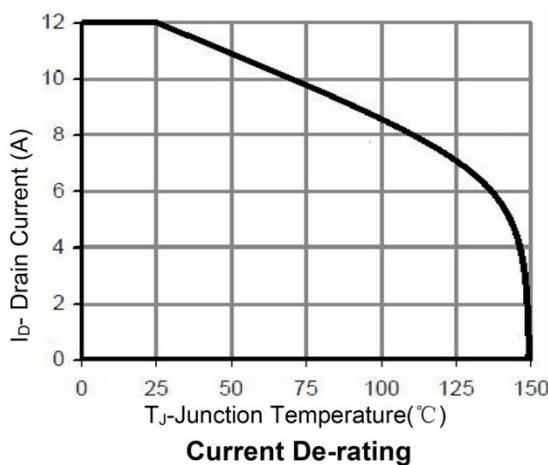
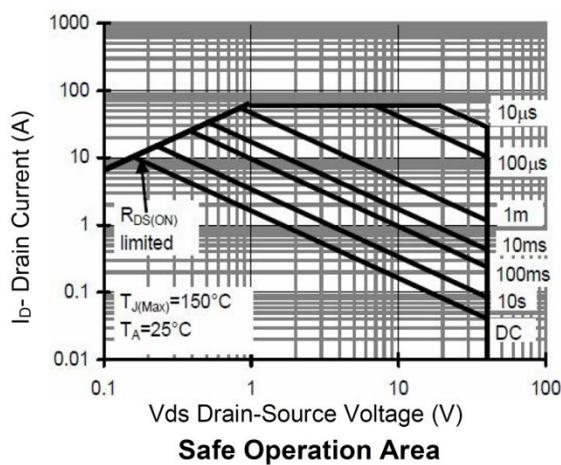
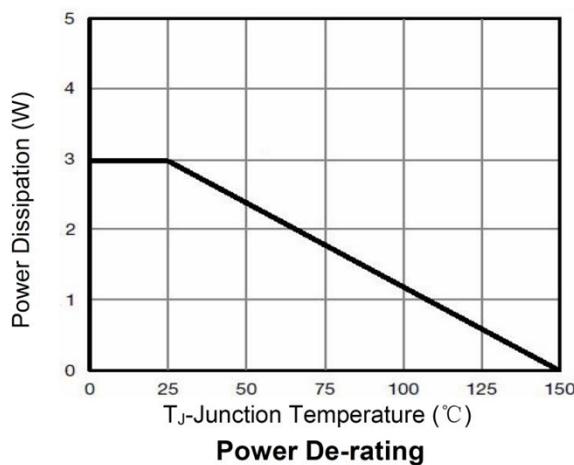
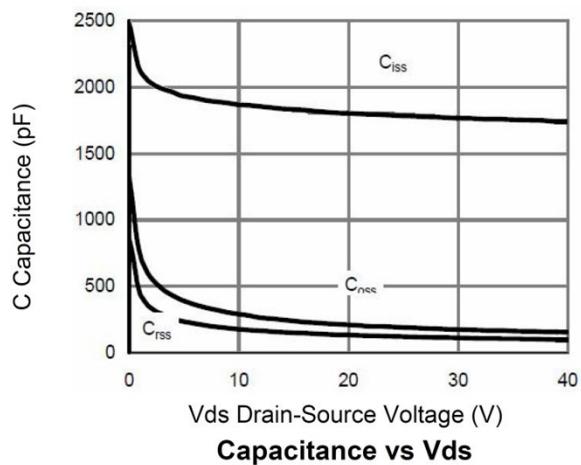


- Switch Time Test Circuit

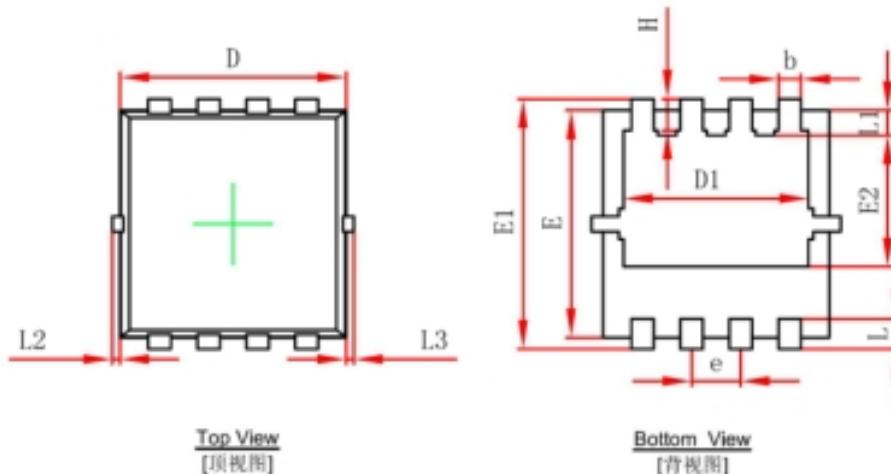


Typical Characteristics





PDFNWB3.3×3.3-8L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.			0.006 REF.
A2	0~0.05			0~0.002
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100			0~0.004
L3	0~0.100			0~0.004
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°